Learning Outcomes

This chapter deals with the construction and operating characteristics of transistors, depending upon how they are connected into a circuit. The basics of semiconductor materials and their application to diodes is covered in *Fundamental Electrical and Electronic Principles*, ISBN 9780750687379, 2008, Chapter 9.

1. The Bipolar Junction Transistor (BJT)

This is a three-layer device where the semiconductor is doped so as to produce a ‘sandwich’ of either two n-type layers with a p-type layer between them, or two p-type layers with an n-type layer between them. The former is known as an npn transistor and the latter as a pnp transistor. The term bipolar refers to the fact that conduction within the device is due to the movement of both positive and negative charge carriers (holes and electrons). Both forms of BJT are illustrated in Fig. 1.

From Fig. 1 it may be seen that the transistor has two p-n junctions, each of which will have the same characteristics as a p-n junction diode. The middle layer of the ‘sandwich’ is much narrower and more lightly doped than the two outer layers.

![Fig. 1](image-url)
Since the device has three layers then it is possible to make three electrical connections to it, i.e. it is a three-terminal device. In addition, it is possible to connect external sources of emf so as to either forward or reverse bias the two internal p-n junctions. The three layers are named the emitter, base and collector, and the action of an npn transistor is illustrated in Fig. 2.

Battery $B_1$ forward biases the emitter-base junction (positive to ‘p’ and negative to ‘n’), whilst the collector-base junction is reversed biased by battery $B_2$. The effect of $B_1$ is to accelerate free electrons from the emitter towards the base. Since the base region is relatively narrow and lightly doped, the vast majority (over 95%) of these electrons will pass straight through the base and cross the second junction into the collector region. Once they reach the collector they will be attracted by the positive potential provided by battery $B_2$, and flow to this battery. The small percentage of the emitter electrons that recombine with holes in the base will be replaced by electron-hole pairs, the electrons from which will leave the base and flow out to the positive plate of $B_1$.

Applying Kirchhoff’s current law to the circuit it may be seen that

$$I_E = I_C + I_B \text{ amp}$$

(1)

This equation will always hold true regardless of the way in which the transistor is connected into a circuit, and could be said to describe normal transistor action. It may also be seen that in Fig. 2 the connection to the base is a common point in the external circuit, and when the transistor is connected in this way it is said to be connected in the common base configuration.

For obvious reasons, the depiction of the transistor in the form of Fig. 2 is not convenient when drawing circuit diagrams, and the circuit symbol for an npn transistor and its use for the circuit of Fig. 2 are shown in Fig. 3.
In the circuit symbol for a transistor the arrowhead indicating the emitter always points in the direction of conventional current flow. This is the same convention as used with the junction diode symbol. It should also be noted that in Figs. 2 and 3(b) the current arrows are actually indicating the direction of electron flow, but if all of these arrows were reversed, the relationship $I_E = I_C + I_B$ would still be true. In Fig. 3(b) the current arrows indicate conventional current flow.

The action of a pnp transistor would be similar to that just described except that electron flow within the transistor would be replaced by holes, and the polarities of the two batteries would have to be reversed to maintain the original biasing conditions for the two p-n junctions. In addition, the circuit symbol for a pnp transistor would have the emitter arrow pointing in the opposite direction to that for an npn transistor as shown in Fig. 4.

---

### 2 Transistor Circuit Configurations

Since the transistor is a three-terminal device there are three possible ways of connecting it into a circuit. These are known as common base, common emitter and common collector configurations, and are shown in Fig. 5.
The characteristics and behaviour of the transistor vary depending upon which configuration is used. The most commonly used configuration is common emitter. The common collector configuration is used for specialised applications and a transistor connected in this way is more normally referred to as an emitter follower.

3 BJT Common Emitter Characteristics

A circuit suitable for obtaining the various characteristics for a common emitter connected transistor is shown in Fig. 6.

Battery $V_{BB}$ supplies the forward bias for the base-emitter junction, whilst $V_{CC}$ reverse biases the collector-emitter junction. The different characteristics are obtained as follows.

**Input Characteristic**  The collector-emitter voltage, $V_{CE}$, is set to a predetermined value by means of $RV_2$. The input base-emitter voltage, $V_{BE}$, is then varied in steps and the corresponding values of base current, $I_B$, noted. Since we are dealing with a forward-biased p-n junction it is no surprise that the input characteristic is the same as for a forward-biased junction diode, as shown in Fig. 7.

The input resistance of the diode, $R_{IN}$, is defined as

$$R_{IN} = \frac{\delta V_{BE}}{\delta I_B} \text{ ohm, with } V_{CE} \text{ constant}$$  (2)
A typical value for $R_{\text{IN}}$ would be between 1000 and 1500 ohm.

**Output Characteristics**  For this test $I_B$ is set to a fixed value using $RV_1$; $V_{CE}$ is varied in steps by means of $RV_2$ and the corresponding values of $I_C$ noted. This procedure is repeated for a number of different fixed values of $I_B$. From the results obtained a family of output characteristics can be plotted as shown in Fig. 8.

Note that, for the sake of clarity, the height of the characteristic for $I_B = 0$ has been exaggerated. Since there is zero input current the only current that can flow is the reverse leakage current across the collector-emitter junction. Since this current will be in the order of a
few microamps, if this characteristic was drawn to the same scale as the axis for $I_C$, it would virtually merge with the horizontal axis. This current is referred to as $I_{CEO}$.

The output characteristics of the transistor are the most useful, since they may be used not only to determine certain parameters of the transistor, but can also be used to predict the behaviour of an amplifier circuit. The output resistance, $R_{OUT}$, of the transistor is defined as

$$R_{OUT} = \frac{\delta V_{CE}}{\delta I_C} \text{ ohm, with } I_B \text{ constant} \quad (3)$$

It is essential to specify the value of base current in this case, since it may be seen that the slope of the characteristics changes with base current. Typical values for $R_{OUT}$ range from 5 kΩ to 100 kΩ.

The large signal or d.c. current gain of the transistor, $h_{FE}$, is defined as

$$h_{FE} = \frac{\delta I_C}{\delta I_B} \text{, with } V_{CE} \text{ constant} \quad (4)$$

This parameter of the transistor may also be obtained from the output characteristics. In Fig. 8, the vertical dotted line represents $V_{CE}$ constant at 5 V. From the intersections of this line with the graphs for $I_B = 20 \mu A$ and $I_B = 100 A$ we can determine the total change in collector current, $\delta I_C$, for the corresponding change in base current, $\delta I_B$, which in this case is 80 A. This relationship between $I_C$ and $I_B$ may also be obtained by plotting the transfer or mutual characteristic as follows.

**Transfer Characteristic** For this test the collector voltage, $V_{CE}$, is maintained constant. The base current is varied in steps, and the corresponding values of collector current noted. These results yield the graph shown in Fig. 9.

Typical values for $h_{FE}$ can range from 10 to 1000.
**Worked Example 1**

Q The input and output characteristics for a certain transistor are as shown in Fig. 10.

Using these characteristics determine the following transistor parameters (a) input resistance, (b) output resistance at a base current of 80 μA, and (c) large signal current gain with \( V_{CE} \) constant at 5 V.

A

(a) Using the linear portion of the input characteristic, for a change in \( V_{BE} \) of 85 mV the corresponding change of \( I_B \) is 88 μA. Hence,

\[
R_{IN} = \frac{\delta V_{BE}}{\delta I_B} \text{ ohm} = \frac{85 \times 10^{-3}}{88 \times 10^{-6}}
\]

and \( R_{IN} = 966 \Omega \text{ Ans} \)
(b) From the output characteristic for \( I_B = 80 \mu A \), a change of \( V_{CE} \) from 8V to 1.4V results in a corresponding change in \( I_C \) from 5.2mA to 4mA. Thus,

\[
\delta V_{CE} = 6.6 \text{ V}; \text{ and } \delta I_C = 1.2 \text{ mA}
\]

\[
R_{\text{OUT}} = \frac{\delta V_{CE}}{\delta I_C} \text{ ohm} = \frac{6.6}{1.2 \times 10^{-3}}
\]

and \( R_{\text{OUT}} = 5.5 \text{ k}\Omega \) Ans

(c) A vertical line at \( V_{CE} = 5V \) (i.e. \( V_{CE} \) constant at this value) intersects the graphs for \( I_B = 140\mu A \) and \( I_B = 20\mu A \) at \( I_C = 8.3 \text{ mA} \) and \( I_C = 1.2 \text{ mA} \) respectively. Thus, \( \delta I_C = (8.3 - 1.2) \text{ mA} = 7.1 \text{ mA} \); and

\[
\delta I_B = (140 - 20)\mu A = 120 \mu A
\]

\[
h_{FE} = \frac{\delta I_C}{\delta I_B} = \frac{7.1 \times 10^{-3}}{120 \times 10^{-6}}
\]

and \( h_{FE} = 59 \) Ans

4 BJT Common Base Characteristics

Using the circuit of Fig. 11, and adopting a similar procedure to that for the common emitter circuit in the previous section (in this case, wherever emitter was specified you now substitute base), the characteristics for this configuration may be obtained.

**Input Characteristic** This will be of the same shape as that obtained for the common emitter configuration since it is the same reverse-biased junction. The essential difference is that the input current is now the emitter current instead of the base current. This will have a considerable effect on the value of the transistor input resistance, \( R_{\text{IN}} \), which is defined as

\[
R_{\text{IN}} = \frac{\delta V_{EB}}{\delta I_E} \text{ with } V_{CB} \text{ constant}
\]

The input characteristic is shown in Fig. 12.

**Output Characteristics** A typical family of output characteristics for a common base connected transistor is shown in Fig. 13.
It may be seen that in this case the graphs are almost horizontal, so that the output resistance will be of a high value, typically in megohms, where

\[ R_{OUT} = \frac{\delta V_{CB}}{\delta I} \text{ ohm, with } I_E \text{ constant} \]  

(6)

The transistor current gain, \( h_{FB} \), is defined as

\[ h_{FB} = \frac{\delta I_C}{\delta I_E} \text{ with } V_{CB} \text{ constant} \]  

(7)

This parameter may also be obtained from the output characteristics as in the case of the common emitter connection, or from the transfer characteristic as follows.

*Transfer Characteristic* A plot of collector current versus emitter current is shown in Fig. 14. Since both current scales are the same, and
the slope of the graph is just less than 45°, then it can be appreciated that the current gain must be less than unity. Typical values for $h_{FB}$ are in the range 0.95 to 0.996.

Worked Example 2

Q The characteristics for a transistor connected in common base configuration are as shown in Fig. 15. Using these characteristics determine (a) the transistor current gain for a collector voltage of 5V, (b) its output resistance, and (c) its input resistance.

A

(a) On the output characteristics, a vertical line is drawn at $V_{CB} = 5$V, and where this line intersects the graphs for $I_E = 4$ mA and $I_E = 1$ mA, the corresponding values for $I_C$ are 3.93 mA and 0.95 mA respectively.

Thus $\delta I_C = 2.98$ mA; and $\delta I_E = 3.25$ mA

and $h_{FB} = \frac{\delta I_C}{\delta I_E} = \frac{2.98}{3.25} = 0.917$ Ans

(b) Since all of the output characteristics have virtually the same slope it does not matter which one is used to determine the output resistance. Thus, from the graph where $I_E = 3$ mA, for the change of $\delta V_{CB} = 10$V, the corresponding change $\delta I_E = 0.1$ mA.

$R_{OUT} = \frac{\delta V_{CB}}{\delta I_E}$ ohm = $\frac{10}{0.1 \times 10^{-3}}$

$R_{OUT} = 100$ k$\Omega$ Ans

(c) From the input characteristic, a change $\delta V_{EB} = 0.2$V results in a corresponding change $\delta I_E = 3$ mA.

$R_{IN} = \frac{\delta V_{EB}}{\delta I_E}$ ohm = $\frac{0.2}{3 \times 10^{-3}}$

$R_{IN} = 66.7$ $\Omega$ Ans
From equation (1) we know that regardless of which configuration is used the relationship \( I_E = I_C + I_B \) is true. This equation may be rewritten in terms of the corresponding changes in these three currents, as follows

\[
\delta I_E = \delta I_C + \delta I_B \\
\text{so,} \quad \frac{\delta I_E}{\delta I_C} = \frac{\delta I_C}{\delta I_C} + \frac{\delta I_B}{\delta I_C} = 1 + \frac{\delta I_B}{\delta I_C} \quad \text{(1)}
\]

Now, from equation (7) we can say that \( \frac{\delta I_E}{\delta I_C} = \frac{1}{h_{FB}} \)
and, from equation (4) we can say that \( \frac{\delta I_B}{\delta I_C} = \frac{1}{h_{FE}} \)

substituting these into [1] above yields

\[
\frac{1}{h_{FB}} = \frac{1}{h_{FE}} + 1 = \frac{1 + h_{FE}}{h_{FE}}
\]

so, \( h_{FB} = \frac{h_{FE}}{1 + h_{FE}} \) (8)

similary, \( h_{FE} = \frac{h_{FB}}{1 - h_{FB}} \) (9)

Provided that we know, from manufacturer’s data, the value of either \( h_{FE} \) or \( h_{FB} \) then we can calculate the transistor current gain in either configuration.

The main parameters of a BJT connected in the three different configurations are summarised in Table 1.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>( R_{IN} )</th>
<th>( R_{OUT} )</th>
<th>( h_F )</th>
</tr>
</thead>
<tbody>
<tr>
<td>common emitter</td>
<td>Medium</td>
<td>Medium</td>
<td>10–1000</td>
</tr>
<tr>
<td>common base</td>
<td>Low</td>
<td>High</td>
<td>&lt;1</td>
</tr>
<tr>
<td>emitter follower</td>
<td>High</td>
<td>Low</td>
<td>&lt;1</td>
</tr>
</tbody>
</table>

6 The Unipolar Junction Transistor (UJT)

The conduction in this device relies solely on the movement of either electrons or holes, and not the combination of both; hence the name unipolar. In addition, the current flow through it is controlled by the application of an electric field, so it is more commonly referred to as a field effect transistor or FET.

There are two main types of FET: the junction gate (JUGFET) which is usually simply called a FET, and the insulated gate (IGFET) which is more often called a MOSFET or simply a MOST.

7 The JUGFET

This device consists of a bar of either n- or p-type silicon into which is diffused two regions of the opposite type of semiconductor. Since electrons are more mobile than holes an n-type bar is more common. This is called an n-channel JUGFET, and is illustrated in Fig. 16.

The n-type bar is known as the channel (through which current can flow). Considering Fig. 16, the effect of \( V_{DS} \) is to cause electrons
to flow from left to right through the channel. For this reason the connection at the left-hand end is called the source, and at the other end is the drain. The two p regions are connected together, and the connection here is called the gate. The gate-source junction is reversed biased by $V_{GS}$ which produces a depletion region in the channel. The shape and size of this depletion region depends upon two factors. The value of $V_{GS}$ determines the extent to which the depletion region extends into the channel. In addition, the electric field through the channel due to $V_{DS}$ will be strongest at the drain end. This will have the effect of increasing the width of the depletion regions towards this end of the channel, resulting in the wedge shape shown in Fig. 16.

The current flow through the FET is therefore determined by the effective length and cross-section of the conducting channel between the depletion regions. This may be compared to controlling the flow of water through a hosepipe by squeezing it. The circuit symbols for both n-channel and p-channel FETs are shown in Fig. 17.

**Fig. 16**

**Fig. 17**

# 8 n-channel JUGFET Characteristics

These characteristics may be obtained in a similar manner to that described for the BJT. However, in the case of the FET, since the gate-source junction is a reverse-biased p-n junction the gate draws negligible current (leakage current only) and the resistance of this junction will be in the order of tens of megohm. For this reason an
input characteristic is not relevant. Typical output and mutual transfer characteristics are shown in Fig. 18.

![Figure 18](image)

(a) output characteristics

(b) transfer characteristics

From the output characteristics it may be seen that variation of $V_{DS}$ from zero to a value equal to $V_p$ volts causes considerable variation of drain current, $I_D$. The value $V_p$ is called the pinch-off voltage because when $V_{DS}$ reaches this value the depletion regions at the drain end of the channel almost meet each other. This section of the characteristics is known as the ohmic or resistive region. As $V_{DS}$ is increased beyond this value, $I_D$ becomes almost independent of $V_{DS}$. $I_{DSS}$ is the drain-source saturation current which is defined later. The dotted portions at high values of drain-source voltage represent the dramatic increase of current due to avalanche breakdown in the p-n junction. For obvious reasons this condition is to be avoided in practice. The FET is normally operated with $V_{DS} > V_p$, and the bias voltage $V_{GS}$ is normally less than or equal to zero.

The reasons for the shape of the output characteristics are illustrated in Figs. 19(a) to (c) for the condition where $V_{GS} = 0$.

From Fig. 19 it may be seen that the dimensions of the conducting channel for $V_{DS} > V_p$ remain virtually constant, hence the current also stays sensibly constant. Although not shown in this series of diagrams, the increase of the negative potential to the gate electrode will also contribute to the narrowing of the conducting channel, and this is clearly demonstrated by the family of output characteristics. The application of a negative potential to the gate therefore reduces (or depletes) the drain current below $I_{DSS}$, and the FET is said to be operating in depletion mode. This is the normal way in which the device is used. It is not normally operated with the gate potential greater than about 0.5 V since this will forward bias the p-n junction, which will then draw significant current into the gate electrode.
9 JUGFET Parameters

There are three main parameters associated with the FET.

**Drain-source Saturation Current** \( (I_{DSS}) \)  This is defined as the drain current that will flow when \( V_{GS} = 0 \) V and \( V_{DS} > V_P \) volt. This will normally be the highest value of drain current flowing.
**Drain-source Resistance** ($r_{DS}$)  This parameter is defined as the ratio of drain-source voltage to drain-source current for a given value (often 0 V) of gate-source voltage. Thus

$$r_{DS} = \frac{\delta V_{DS}}{\delta I_{DS}} \text{ ohm, with } V_{GS} \text{ constant}$$

This parameter may be obtained from the output characteristics, and typical values would be in the low to mid kilohm range.

**Mutual Conductance or Transconductance** ($g_m$)  This parameter may be obtained from the transfer characteristic of Fig. 18(b), where it may be seen that the slope of the graph at any point is given by the value of drain current at that point divided by the corresponding value of gate-source voltage. Thus

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \text{ siemen, with } V_{DS} \text{ constant}$$

Typical values for $g_m$ range from 0.05 mS to 10 mS. A value for $g_m$ may also be obtained from the output characteristics in a similar manner to that used to obtain $h_F$ for the BJT.

---

**Worked Example 3**

**Q**  The output characteristics for a FET are shown in Fig. 20. Assuming $V_{DS} = 15$ V and $V_{GS} = -0.4$ V, determine the values for (a) $r_{DS}$ and (b) $g_m$.

![Fig. 20]
### A

(a) With $V_{GS} = -0.4\,\text{V}$ and $\delta V_{GS} = (20 - 10) = 10\,\text{V}$ the corresponding change in drain current, $\delta I_D = (2.7 - 2.55)\,\text{mA} = 0.15\,\text{mA}$

$$r_{DS} = \frac{\delta V_{GS}}{\delta I_D}\,\text{ohm} = \frac{10}{0.15} = 66.7\,\text{kΩ} \quad \text{Ans}$$

(b) For $V_{DS} = 15\,\text{V}$ and $\delta V_{GS} = 0 - (-1) = 1\,\text{V}$ the corresponding change in drain current, $\delta I_D = (4.4 - 0.6)\,\text{mA} = 3.8\,\text{mA}$

$$g_m = \frac{\delta I_D}{\delta V_{GS}}\,\text{siemen} = 3.8 \times 10^{-3}$$

$$g_m = 3.8\,\text{mS} \quad \text{Ans}$$

### 10 The Metal-Oxide-Semiconductor Transistor (MOSFET)

This device is an insulated gate FET (IGFET) as previously stated. It consists of a lightly doped p-type substrate into which are diffused two heavily doped n-type regions which form the source and drain. On the upper surface is deposited a very thin layer of silicon oxide which acts as an insulating layer. External electrical connections to the source and drain regions are via holes or windows left in the oxide layer. A cross-section of the transistor is shown in Fig. 21.

When a positive potential is applied to the gate terminal the resulting electric field will attract electrons (from thermally generated electron-hole pairs) towards the top surface of the substrate, and repel holes away from it. As the gate potential is increased more electrons are attracted towards the upper surface until, at a voltage known as the threshold voltage, $V_T$, a conducting or inversion channel of n-type semiconductor is induced between source and drain. For this reason this device is called an n-channel MOSFET. A typical value for $V_T$ is between 2 V and 4 V. When the gate potential is increased beyond $V_T$ even more electrons are attracted into the conducting channel. This will have the effect of increasing or enhancing the drain current, and
this mode of operation is known as enhancement mode. If an n-type substrate is used with p-type drain and source, and the polarities at the three electrodes are reversed, then a p-type channel is induced, and the device is called a p-channel MOSFET.

The circuit symbols for both types are shown in Fig. 22. Note that the channel between source and drain is shown as a broken line, because until $V_{GS} > V_T$ the transistor will not conduct. In addition, although there is never any electrical connection made to the substrate, it is always shown on the circuit symbol, and the arrowhead indicates which type of channel is employed.

![Circuit symbols for both types](image)

Fig. 22

Typical characteristics for an n-channel enhancement mode MOSFET are shown in Fig. 23.

![Typical characteristics](image)

Fig. 23

11 Depletion Mode MOSFET

The construction of this device is very similar to that for the enhancement mode device but with the exception that, during the manufacturing process, a conducting channel is diffused between source and drain. This is referred to as the initial channel, and the physical arrangement is illustrated in Fig. 24(a).

Fig. 24(b) is used to describe the operation, as follows. Since the source and drain are joined by a conducting channel then drain current can flow even when $V_{GS}$ is zero. When the gate potential is made negative, the electric field will attract holes from the substrate into
the n-channel, where recombinations will occur. Thus the number of free electrons in the n-channel is reduced or depleted, and the drain current will be reduced. It should be noted that if the gate is made positive then more electrons will be attracted into the channel and drain current will increase. Thus this device may be used in either depletion or enhancement mode. The circuit symbols for both n- and p-channel devices are shown in Fig. 25. In these cases the conducting channel being a permanent feature, it is shown by a continuous line.

Typical output and transfer characteristics for the device are shown in Fig. 26.

Typical values for the MOSFET parameters are:

Drain-source resistance, \( r_D = 1 \) to \( 50 \) k\( \Omega \)
Gate input resistance, \( r_G > 10 \) G\( \Omega \)
Mutual conductance, \( g_m = 0.1 \) to \( 25 \) mS
### 12 Comparison of FETs with BJTs

FETs differ from BJTs in a number of important ways.

1. Conduction in FETs consists only of majority carriers. Hence the general title of unipolar junction transistors.
2. BJTs are current-operated devices whereas conduction in FETs is controlled by an electric field.
3. As a consequence of 2 above, FETs have an extremely high input resistance, and (theoretically at least) draw no current at the input, i.e., there is negligible loading effect on any input source.
4. FETs are simpler to manufacture and occupy less physical space. This can be particularly important for integrated circuit (IC) chips, where the size and hence possible density of devices accommodated on the chip can be vital.

### Summary of Equations

**BJT – normal transistor action:** $I_E = I_C + I_B \text{ amp or } I_e = I_c + I_b \text{ amp}$

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{IN} = \frac{\delta V_{BE}}{\delta I_B}$ ohm, with $V_{CE}$ constant</td>
<td>Common emitter BJT: $I_C = I_e$</td>
</tr>
<tr>
<td>$R_{OUT} = \frac{\delta V_{CE}}{\delta I_C}$ ohm, with $I_B$ constant</td>
<td></td>
</tr>
<tr>
<td>$h_{FE} = \frac{\delta I_C}{\delta I_B}$ with, $V_{CE}$ constant</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{IN} = \frac{\delta V_{EB}}{\delta I_E}$ with, $V_{CB}$ constant</td>
<td>Common base BJT: $I_E = I_B$</td>
</tr>
<tr>
<td>$R_{OUT} = \frac{\delta V_{CB}}{\delta I_C}$ with, $I_E$ constant</td>
<td></td>
</tr>
<tr>
<td>$h_{FB} = \frac{\delta I_C}{\delta I_B}$ with, $V_{CB}$ constant</td>
<td></td>
</tr>
</tbody>
</table>

**Relationship between $h_{FE}$ and $h_{FB}$:** $h_{FE} = \frac{h_{FB}}{1 - h_{FB}}$

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$h_{FB} = \frac{h_{FE}}{1 + h_{FE}}$</td>
<td></td>
</tr>
</tbody>
</table>

**FET parameters:** $r_{DS} = \frac{\delta V_{DS}}{\delta I_D}$ ohm, with $V_{GS}$ constant

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m = \frac{\delta I_D}{\delta V_{GS}}$ siemens, with $V_{DS}$ constant</td>
<td></td>
</tr>
</tbody>
</table>
**Assignment Questions**

1. A common emitter connected transistor has characteristics as shown in Fig. 27. Using these graphs determine (a) transistor output resistance for a base current of 80 µA, (b) transistor input resistance, and (c) transistor current gain for $V_{CE} = 6$ V.

2. For the common base characteristics shown in Fig. 28 determine (a) transistor current gain, (b) output resistance, and (c) the corresponding value of transistor current gain if the transistor was connected in common emitter configuration.

3. A FET has characteristics as given in Table 2 below. Plot these characteristics and hence determine the parameters (a) drain-source resistance, and (b) mutual conductance for $V_{GS} = 12$ V.

![Fig. 27](image-url)
### Assignment Questions

**Fig. 28**

![Graph showing the relationship between \( V_{DS} \) and \( I_{DS} \).](image)

**Table 2**

<table>
<thead>
<tr>
<th>( V_{GS} ) (V)</th>
<th>( I_{DS} ) (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{GS} = -2.5 \text{V} )</td>
<td>( V_{GS} = -2.0 \text{V} )</td>
</tr>
<tr>
<td>4</td>
<td>0.6</td>
</tr>
<tr>
<td>16</td>
<td>1.0</td>
</tr>
<tr>
<td>24</td>
<td>1.4</td>
</tr>
</tbody>
</table>
Suggested Practical Assignments

For the following assignments it is left to the student (under the guidance of the teacher) to select appropriate apparatus. The circuit diagrams and method to follow are to be found in the relevant sections (3, 4 and 9). For each assignment all results should be tabulated and the corresponding graphs plotted.

Assignment 1

To obtain the output and input characteristics for a BJT when connected (a) in common base, and (b) in common emitter configuration. From the plotted graphs determine the transistor parameters in each configuration, and compare the relationship between transistor gain of the two configurations with the theoretical value.

Assignment 2

To obtain the output and transfer characteristics for a FET, and from the plotted graphs determine the transistor parameters.
# Answers to Assignment Questions

1. (a) 1.58 kΩ  
   (b) 360 Ω  
   (c) 212

2. (a) 0.997  
   (b) 200 kΩ  
   (c) 332

3. (a) 7.7 kΩ  
   (b) 2.7 ms